UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,634	12/17/1999	DAVID K. VAVRO	ITL.0286US (P7814)	9115

21906 7590 12/01/2008

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	PAPER NUMBER
2181	
MAIL DATE	DELIVERY MODE
12/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/465,634
Filing Date: December 17, 1999
Appellant(s): VAVRO ET AL.

Timothy N. Trop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/17/2008 appealing from the Office action mailed 12/12/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Appeal No. 2003-1635, decision mailed on September 17, 2004, for this application.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: Claims 1-4, 6-7, 9-16, and 18-24 are rejected under 35 U.S.C. 103(a) as being *unpatentable* over Balmer, U.S. Patent No. 5,197,140.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Balmer, U.S. Patent No. 5,197,140, issued March 23, 1993.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6, 7, 9-16, and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balmer, U.S. Patent No. 5,197,140.

Referring to claim 1, Balmer has taught a digital signal processor comprising:

a programmable, multiply and accumulate mathematical processor (Figure 4, elements 101-103, column 35, lines 39-56, columns 8-11, A multiply and an ALU operation is performed by each processor, elements 101-103, every cycle. An ALU operation is an accumulation.);

an input processor that processes input signals to the digital signal processor (Figures 2, 4, and 17, transfer processor and frame controllers, column 58, line 60- column 59, line 20, column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15. The input processor is the portion of the transfer processor that processes a set of data input instructions from an external memory, see column 11, line 55-column 12, line 12.);

an output processor that processes output signals from the digital signal processor (Figures 2, 4, and 17, transfer processor and frame controllers, column 58, line 60- column 59, line 20, column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15, The output processor is the portion of the transfer processor that processes a set of data output instructions to an external memory, see column 11, line 55-column 12, line 12. Column 25, lines 20-34);

a master processor that controls said mathematical processor, said input processor and said output processor provides the timing for the other processors (Figures 2, 4, and 17, master processor, column 3, lines 10-17, column 4, line 60-column 5, line 5, column 12, lines 14-34);

a storage to store data from each of said processors so as to be selectively accessible by each of the processors (column 2, line 67-column 3, line 17, column 47- column 7, line 47); and

wherein each of said processors has an instruction set (The mathematical processor processes a set of low-level instructions, see column 14, line 47-column 15, line 18. The master processor processes a set of high-level instructions, including floating point operations, see column 14, line 47-column 15, line

18. The input processor is the portion of the transfer processor that processes a set of data input instructions from an external memory, see column 11, line 55-column 12, line 12. The output processor is the portion of the transfer processor that processes a set of data output instructions to an external memory, see column 11, line 55-column 12, line 12. Column 25, lines 20-34).

Balmer has not specifically taught wherein each of said processors has a different instruction set than the other processors. However, each processor has a different set of required tasks to make the system operate as described. A customized processor with a unique instruction set that is only able to execute the required tasks is able to perform in an optimized and efficient manner. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to customize each of the processors for their required tasks such that each processor would have its own unique optimized instruction set for the desirable purpose of increasing processor efficiency.

Referring to claim 2, Balmer has taught the digital signal processor of claim 1 further including a random access memory processor that stores intermediate calculation results (column 5, lines 47-61, see RAMS).

Referring to claim 3, Balmer has taught the digital signal processor of claim 2 including a bus coupling each of said processors to said storage (column 6, lines 39-52).

Referring to claim 4, Balmer has taught the digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations (Figures 2,4, and 17, transfer processor and frame controllers, column 58, line 60-column 59, line 20 column 3, lines 10-17, column 11, line 55-column 12, line 12, column 4, line 60-column 5, line 13, column 7, lines 8-15).

Referring to claim 6, Balmer has taught the digital signal processor of claim 1 wherein said processors communicate with one another through said storage (column 2, line 67-column 3, line 17, column 47-column 7, line 47).

Referring to claim 7, Balmer has taught the digital signal processor of claim 1, as described above. Balmer has not taught wherein each of said processors use very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for several instructions of Balmer to be issued at once. Furthermore, by the nature of very long instruction words, the

compiler would have only combined instructions that are not dependent upon one another. Issuing multiple independent instructions at once would have speed up the overall execution time of the processor by reducing the idle time of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the very long instruction word format for instructions issued to the plural processors of Balmer in order to increase speed and efficiency of those processors. Official notice has been taken.

Referring to claim 9, Balmer has taught the digital signal processor of claim 1 wherein said master processor waits for the input processor to complete a given operation (column 59, lines 12-20, column 1l, line 55-column 12, line l2).

Referring to claim 10, Balmer has taught the digital signal processor of claim 1 wherein each of said processors includes its own random access memory (column 5, lines 47-61, see RAMS).

Referring to claim 11, Balmer has taught the digital signal processor of claim 1, as described above, and wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register (column 43, line 50-column 45, line 52, saving the interrupt state).

Referring to claim 12, Balmer has taught the digital signal processor of claim 11, as described above, and wherein said input processor causes the automatic transfer of data (column 43, line 50-column 45, line 52, When an interrupt occurs, see "Packet Request", the state is saved.).

Referring to claim 13, Balmer has taught the digital signal processor of claim 11, as described above, and wherein said mathematical processor causes said data to be transferred from one register to another (column 43, line 50-column 45, line 52).

Referring to claim 14, Balmer has taught the digital signal processor of claim 1 including a mathematical processor which is pipelined (column 39, lines 20-45).

Referring to claim 15, Balmer has taught the digital signal processor of claim 1 wherein said mathematical processor is a multi-cycled mathematical processor (column 39, lines 20-45, where an operation takes multiple cycles to complete. In this case a pipelined processor takes multiple cycles to complete.).

Claim 16 does not recite limitations above the claimed invention set forth in claim 1 and is therefore rejected for the same reasons set forth in the rejection of claim 1 above.

Claims 18-20 do not recite limitations above the claimed invention set forth in claims 11- 13 and are therefore rejected for the same reasons set forth in the rejection of claims 11 -13 above.

Referring to claim 21, Balmer has taught storing a bit which indicates which processor may control said automatic transfer of data from one register to another (column 50, lines 15-35; column 44, lines 34-67).

Claim 22 does not recite limitations above the claimed invention set forth in claim 14 and is therefore rejected for the same reasons set forth in the rejection of claim 14 above.

Claims 23 and 24 do not recite limitations above the claimed invention set forth in claim 15 and are therefore rejected for the same reasons set forth in the rejection of claim 15 above.

(10) Response to Argument

First ground of rejection:

Claims 1-4, 6, 7, 9-16, and 18-24:

Applicant argues the novelty/rejection of the claims, in substance that:

"The cited reference fails to teach using different instruction sets, for each of three processors, as claimed and also fails to suggest using three different types of processors."

These arguments are not found persuasive for the following reasons.

Balmer, in reference to the master processor and the low level/parallel processors (i.e. programmable, multiply and accumulate mathematical processor), states that "[t]he main reason why two different types of processors are necessary is because of the level of processing [Balmer; column 14, lines 47-49]." Balmer goes on to describe that the master processor requires the use of floating point arithmetic, whereas "the low level processors not require floating point arithmetic and thus can be made faster and smaller, which in turn allows more processors to be constructed on a given chip." [Balmer; column 14, 51-60] As would be recognized by one of ordinary skill in the art, processors that execute different operations and are of different types are said to have different instruction sets. Because Balmer explicitly states that the master processor and the low level processor (i.e. programmable, multiply and

accumulate processor) execute different operations, Balmer has explicitly taught that the master processor and the programmable, multiply and accumulate processor have different instructions sets. Balmer is silent on the specific instruction set of the other processors in the system (e.g. input processor and output processor). However, Balmer, as noted above, explains that the motivation for the master processor and low level processor having different instruction sets is that they perform different types of processing and, therefore, require different operations/instruction.

This same motivation applies to the other processors in the system of Balmer (e.g. the input processor and output processor). While Balmer is silent on the instruction sets of these processors, Balmer explains that they perform different types of processing. Specifically, Balmer states that the input processor (i.e. respective portion of transfer processor) processes a set of data input instructions and that the output processor (i.e. respective portion of transfer processor) processes a set of data output instructions [Balmer; column 11, line 55-column 12, line 12. Column 25, lines 20-34]. Because these processors perform different types of processing and, therefore, require different operations/instruction, it would have been obvious for them to have different instruction sets from the other processors in the system. Therefore, the rejection does not use hindsight reasoning, but instead uses motivation explicitly described by Balmer.

(11) Related Proceeding(s) Appendix

Copies of the court or Board decision(s) identified in the Related Appeals and Interferences section of this examiner's answer are provided herein.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted

Benjamin Geib

/Benjamin P Geib/

Examiner, Art Unit 2181

Conferees:

Alford Kindred
/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

Kevin Ellis
/Kevin L Ellis/
Acting SPE of Art Unit 2187